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# Calculation of Gate Capacitance in Metal Oxide Semiconductor Field Effect Transistors

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**Abstract**

In the present work, authors have calculated the inversion layer capacitance and depletion layer capacitance in MOSFET . Depletion layer capacitance is determined by depletion layer thickness ($t_{di}$) where solution of Poisson's equations have an important role.

**Keywords:** Gate Capacitance, MOSFETs.

**Introduction**

The drain current is controlled by applied electric field or gate voltage in MOSFET [1]. The MOSFET is divided in two categories viz enhancement MOSFET and DEMOSFET. DEMOSFET means depletion enhancement MOSFET. DEMOSFET operates in both depletion and enhancement mode. When gate voltage is negative for N channel DEMOSFET, it operates in depletion mode and when gate voltage is positive for N channel DEMOSFET then it operates in enhancement mode. The drain current ($I_d$) flows even when gate source voltage ($V_{gs}$) is zero because a channel exists between drain and source .We apply both negative and positive gate voltages in MOSFET because it is insulated from the channel. The gate ($SiO_2$) and channel form a parallel plate capacitor. When MOSFET operates with positive bias gate voltage, the drain current does not exist even when some positive $V_{ds}$ is applied. In order to obtaine the significant amount of drain current, we need to apply sufficiently high positive gate voltage. This voltage is found to produce a thin layer of free electrons very close to the metal oxide ($SiO_2$) film which stretches all the way from source to drain. This thin layer of p-substrate touching the metal oxide film provides the channel for electrons ( acts like N-type material) is called N-type inversion layer or virtual N-channel. The minimum gate-source voltage which produces this P or N-type inversion layer to start the flow of drain current is called threshold voltage ($V_{gs(th)}$ or $V_{th}$). When $V_{gs} < V_{th}$ then $I_d=0$. Drain current start only when $V_{gs} > V_{th}$ . In this work we determine the inversion layer capacitance ($C_{inv}$) for two different dielectric materials $SiO_2$ and $Si_3N_4$ with dielectric constant 3.9 and 7 respectively. The Poisson's equation is useful for calculating the depletion layer thickness. In turn, depletion thickness $t_{di}$ is helpful in determining the depletion layer capacitance $C_{di}$.

**Objective of the study**

When we explain the MOSFETs features, we should have in mind the various capacitances affects the speed of MOSFETs in different operational mode. Such type of capacitances are parasitic capacitances. Influence of such type of capacitance on MOSFET operation is given by [2-3]. Other type of capacitances are inversion layer capacitance and depletion layer capacitance. The gate of MOSFET can be considered to be a capacitance. The gate voltage of a MOSFET does not increase unless its gate input capacitance is charged and the MOSFET does not turn on until its gate voltage reaches to the gate threshold voltage ($v_{th}$). This threshold voltage is a minimum voltage which creates a conduction channel between source and drain regions [4]. When MOSFET in operation mode, it is essential to calculate the inversion layer capacitance ($C_{inv}$) and depletion layer capacitance ($C_{di}$).

**Review of Literature**

The gate capacitance in MOSFET is important parameter for performance of the devices made by MOSFETs. The parasitic capacitance in MOSFET is calculated by Nebi Caka and Neha Srivastava [2-3]. At present scenario as technology improves, the dimensions of the devices decrease, so there are more challenges created in determining the

parameter of the devices. The dimensions of devices shrink in nano scale such as corbon nanotube field effect transistors. The gate capacitance of carbon nanotube field effect transistor is calculated by H. kumar [5].

$$C_g = e\frac{dN_e}{dV_g}$$

When the bulk material dimensions shrink in nano scale, its features drastically change. So it is very difficult to estimate the charecteristics of the devices. However many charecteristics such as energy band gap, specific heat of nano device are calculated by Hemendra kumar [6].

**Concepts**

We know that if any tiny particle moves, a wave gets associated with it. All these problems are dealt with wave function whoes solution is given by Schroedinger equation.

$$-\frac{\hbar^2}{2m_e}\frac{d^2\psi}{dx^2} + \varphi(x)\psi = E\psi$$

In this paper the Poisson's equation which is useful tool for determining the depletion layer thickness $t_{di}$, the boundary conditions for the Poisson's equation are

$$\frac{d^2\Phi}{dz^2} = \frac{[\rho_{depl}(t) - e\sum N_i\xi^2(t)]}{K_{sc}\mathcal{E}_0}$$

The term dφ/dt from that eqiuation disappears for large depletion layer thickness $t_{di}$ .

**Research Design**

**Calculation of inversion layer capacitance ($C_{inv}$)**

To find the value of $C_{inv}$ , we apply the self consistant solution. The first numerical self consistant calculation for inversion layers were made by Howard and Stern [7].

$$C_{inv} = \frac{eN_{inv}}{F_s}$$

Where $F_s$ is the silicon surface potential given by equation

$$F_s = \frac{e[N_{inv} + N_{depl}]}{K_{sc}\mathcal{E}_0}$$

Thus inversion layer capacitance $C_{inv}$ is given by

$$C_{inv} = \frac{N_{inv}.K_{sc}.\mathcal{E}_0}{N_{inv}+N_{depl}}$$

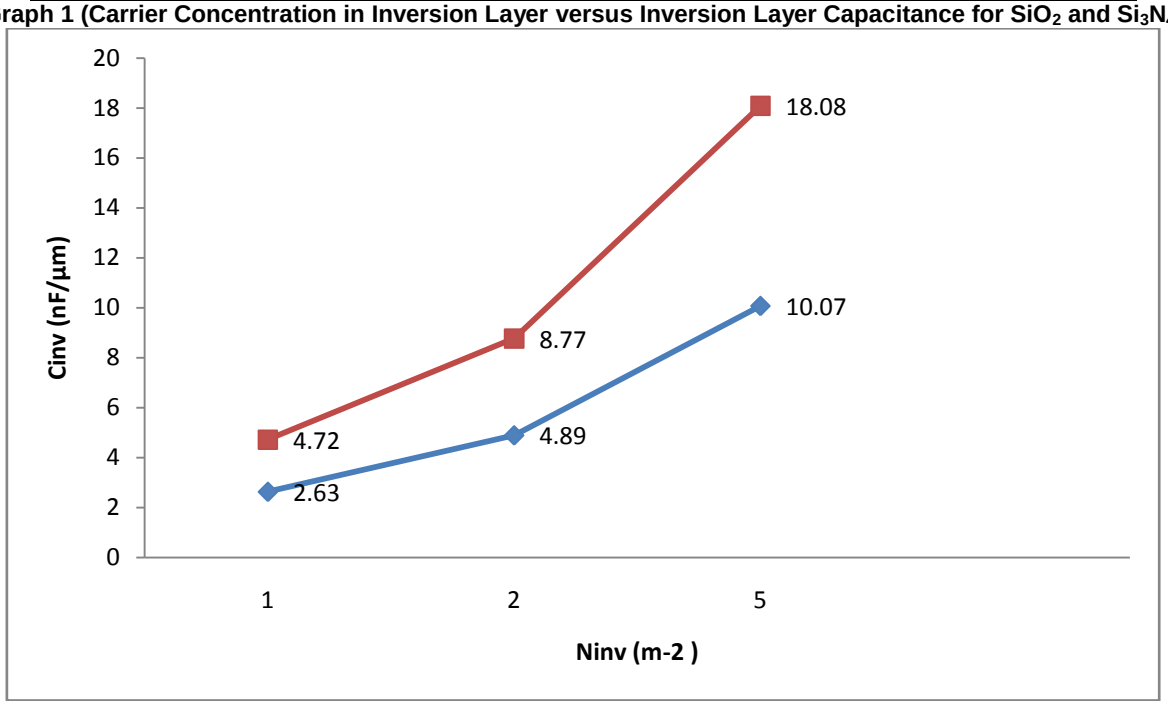
Now we calculate the $C_{inv}$ , the different dielectric materials for $SiO_2$ and $Si_3N_4$ with dielectric constant of these semiconductors ( $K_{sc}$ ) are 3.9 and 7 respectively with given parameters in table 1. The graph is ploted between $C_{inv}$ and $N_{inv}$ as shown in figure 1.

**Table-1**

**Value of $C_{inv}$ with different $N_{inv}$ at constant $N_{depl}$**

| S.No. | $N_{inv}$ ($m^{-2}$) | $N_{depl}$ ($m^{-2}$) | For $SiO_2$ $C_{inv}$ (nF/μm) | For $Si_3N_4$ $C_{inv}$ (nF/μm) |
|---|---|---|---|---|
| 1 | $1 \times 10^{14}$ | $1.213 \times 10^{15}$ | $2.63 \times 10^{-3}$ | $4.72 \times 10^{-3}$ |
| 2 | $2 \times 10^{14}$ | $1.213 \times 10^{15}$ | $4.89 \times 10^{-3}$ | $8.77 \times 10^{-3}$ |
| 3 | $5 \times 10^{14}$ | $1.213 \times 10^{15}$ | $10.07 \times 10^{-3}$ | $18.08 \times 10^{-3}$ |

**Graph 1 (Carrier Concentration in Inversion Layer versus Inversion Layer Capacitance for $SiO_2$ and $Si_3N_4$)**




**Calculation of Depletion Layer Capacitance ($C_{di}$)**

To calculate the depletion layer capacitance of a MOSFET, we consider the depletion layer thickness ($t_{di}$) first **.** This thickness can be calculated by the charge density of the depletion layer i.e.

$$t_{di} = [2K_{sc}\mathcal{E}_0\Phi_d/e(N_A - N_D)]^{1/2}$$

Where $N_A$ and $N_D$ is the charge density , $\varphi_d$ is effective band bending from the bulk to the surface, apart from the contribution of the inversion layer itself. The boundary conditions for the Poisson's equation

$$\frac{d^2\Phi}{dz^2} = \frac{[\rho_{depl}(t) - e\sum N_i\xi^2(t)]}{K_{sc}\mathcal{E}_0}$$

The term dφ/dt from that eqiuation disappear for large t and its value at the surface be $F_s$ which is useful for considering the inversion layer capacitance. Hence the depletion layer capacitance $C_{di}$ is given by relation

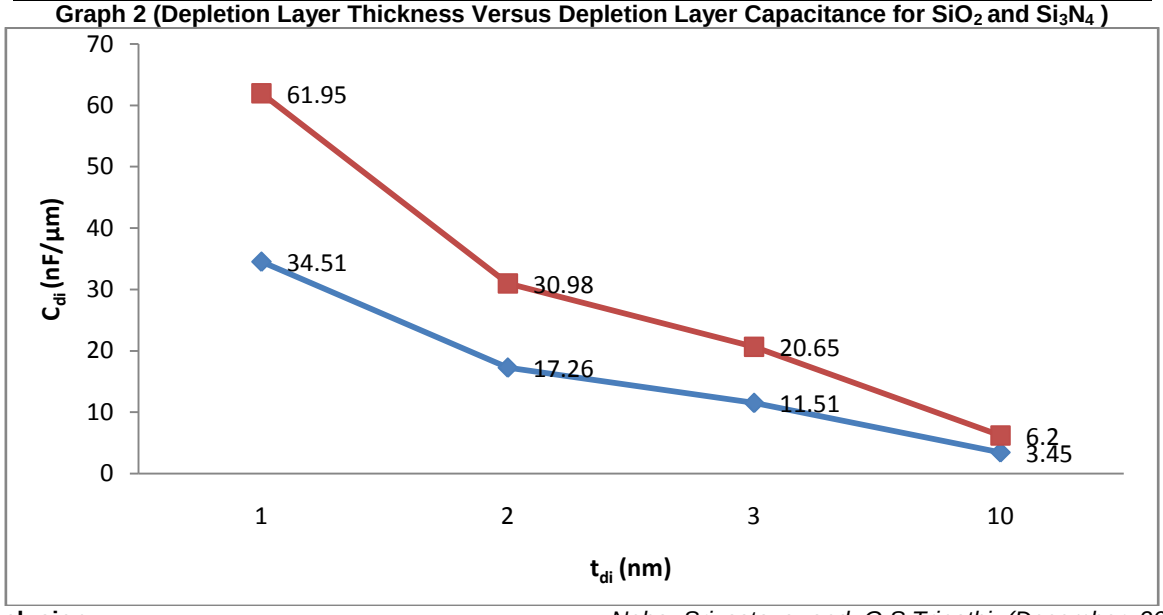
$$C_{di} = \frac{\varepsilon_0 K_{sc}}{t_{di}}$$

Using parameters given in table 2 for two dielectric materials $SiO_2$ and $Si_3N_4$ with dielectric constants ($K_{sc}$) 3.9 and 7 respectively, the graph is ploted between the $C_{di}$ and $t_{di}$ as shown in figure 2.

**Table-2**
**Value of $C_{di}$ at different $t_{di}$**

| S.No. | $T_{di}$ thickness $SiO_2$ & $Si_3N_4$ | $\varepsilon_0$ | For $SiO_2$ $C_{di}$ (nF/μm) | For $Si_3N_4$ $C_{di}$ (nF/μm) |
|---|---|---|---|---|
| 1 | 1.0 nm | 8.85 X $10^{-12}$ F/m Or 8.85 X $10^{-3}$ nF/m | 34.51X $10^6$ | 61.95 X $10^6$ |
| 2 | 2.0 nm | 8.85 X $10^{-12}$ F/m Or 8.85 X $10^{-3}$ nF/m | 17.26X $10^6$ | 30.98 X $10^6$ |
| 3 | 3.0 nm | 8.85 X $10^{-12}$ F/m Or 8.85 X $10^{-3}$ nF/m | 11.51 X $10^6$ | 20.65 X $10^6$ |
| 4 | 10.0 nm | 8.85 X $10^{-12}$ F/m Or 8.85 X $10^{-3}$ nF/m | 3.45 X $10^6$ | 6.20X $10^6$ |

**Graph 2 (Depletion Layer Thickness Versus Depletion Layer Capacitance for $SiO_2$ and $Si_3N_4$ )**




**Conclusion**

From Table 1 we observed a trend that when the inversion layer concentration of carriers increases then the value of inversion layer capacitance also increases. This trend is also shown in the graphical repersention (fig. 1). All these results are obtained at constant depletion layer carrier concentration. It is evident from the table 2 that, the depletion layer capacitance decreases with increase of depletion region thickness $t_{di}$. Hence we conclude that by controlling the depletion layer thickness $t_{di}$ or depletion layer capacitance $C_{di}$, we can change the MOSFET speed and other features.

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